a semiconductor substrate;

at least two semiconductor components provided on the principal surface of the substrate;

electrodes of the at least two components provided on the substrate so as to substantially eliminate the electrical interference between the two semiconductor components;

a first group of through holes, which pass from the principal surface through the backside of the substrate and are provided in respective regions of the substrate under the electrodes;

a first conductor film provided on the side faces of the first group of through holes;

a second group of through holes, which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the components;

a second conductor film provided on the side faces of the second group of through holes; and

a wiring layer, which is provided on the backside of the substrate and is in contact with the first and second conductor films.

REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the present application.

The Examiner's non-final Office Action dated May 29, 2002 has been received and its contents reviewed. Claims 1-7 are pending in the present application of which claims 1 and 6 are independent. By this amendment, claims 1 and 6 have been amended.

Claims 1, 3, 4, and 6 are rejected under 35 U.S.C. §102(b) as anticipated by the newly cited Fujuita et al. reference (U.S. Patent No. 5,485,039 - hereafter Fujita). Further, claims 2, 5, and 7 are rejected under 35 U.S.C. §103(a) as unpatentable over Fujita. These rejections are respectfully traversed at least for the reasons provided below.